VIT Vellore Institute of Technology

Reg. No. : 21BCE1846

Final Assessment Test (FAT) – November/December 2022

Programme	**B.Tech.**	Semester	**Fall Semester 2022-23**
Course Title	**DIGITAL SYSTEMS DESIGN**	Course Code	**BECE102L**
Faculty Name	**Prof. E Manikandan**	Slot	**E1+TE1**
		Class Nbr	**CH2022231001853**
Time	**3 Hours**	Max. Marks	**100**
Answer All Questions			

PART A (7 X 5 Marks)
Answer All questions

1. Obtain the truth table of the following Boolean function (F) and express the function in sum of minterms and product of maxterms. [5]
   F = bd' + acd' + ab'c + a'c'
2. Implement the following Boolean function F together with don't care condition d, using not more than two NOR gates [5]
   F(A, B, C, D) = ∑ (2, 4, 10, 12, 14)
   d(A, B, C, D) = ∑ (0, 1, 5, 8)
3. Draw the CMOS logic circuit for the Boolean expression given below. Assume both the true and complementary inputs are available. [5]
   Y = (ABC + DE + F)
4. Write a test bench for a clock with a time period of 40 units and a duty cycle of 25% (ON TIME =25 % AND OFF TIME =75 %) by using always and initial statements. The value of the clock at time t = 0 should be initialized to 0. [5]
5. Given below is an initial block with procedural assignments. At what simulation time is each statement executed? What are the intermediate and final values of a, b, c, d? [5]

```
initial
begin
a = 1'b0;
b = #10 1'b1;
c = #5 1'b0;
d = #20 {a, b, c};
e=#10 a^b;
end
```

6. Implement the following Boolean expression using a suitable multiplexer. [5]
   F(w,x,y,z) = w'xz'+wyz+x'yz+y'w'z
7. Consider two 4-bit numbers A=$A_3A_2A_1A_0$ and B=$B_3B_2B_1B_0$, write the Verilog code to check whether these two numbers are equal or not using behavioral modeling. [5]

PART B (5 X 10 Marks)
Answer All questions

8. Specify the truth table of an octal (8–bit input to binary 3-bit output) priority encoder. Provide an output V to indicate that at least one of the inputs is present. The input with the highest subscript number has the highest priority. What will be the value of the four outputs if inputs D2 and D6 [10]

are 1 at the same time? Write the Verilog code for the same.

9. Construct a digital logic circuit for 2x2 bit multiplier using half adders. [10]
10. Design a synchronous sequential circuit that generates a sequence 0-2-5-4-7-3 using JK flip-flop. [10]
11. Explain the working of SISO shift register. Write a Verilog HDL code for the same. [10]
12. Implement the following Boolean function with PLA & PAL logic. [10]
    $F(A, B, C, D) = \sum (0, 2, 6, 7, 8, 9, 12, 13, 14)$

PART C (1 X 15 Marks)

Answer <u>All</u> questions

13. Design a sequence detector for '1101' using D flip-flops. Also, draw the state diagram for a sequence detector that outputs a 1 when it detects the final bit in the serial data stream using Moore model. [15]