Reg. No.: 21BCE1896

Name :

VIT

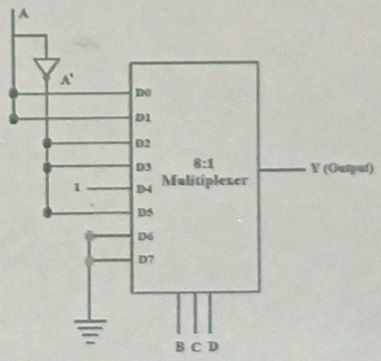
Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

Continuous Assessment Test II – October 2022

Programme	: B.Tech (CSE, CSE(AIR), CSE(CPS), CSE(AI&ML))	Semester	:		FS 2022-23
Course	: Digital System Design	Code	:		BECE102L
		Class Nbr	:		CH2022231001853
Faculty	: Dr.E.MANIKANDAN	Slot	:		E1+TE1
Time	: 90 Minutes	Max. Marks	:		50

Answer ALL the questions

Q. No.	Sub-division	Question Text	Marks
1.		Determine the Boolean function implemented in Fig 1 and implement the same Boolean function using suitable Demultiplexer.	[5+3]
		 **Figure 1**	
2.		Determine whether the given function is an even or odd parity generator and write the Verilog code for the same along with the test bench $f(a, b, c) = ab'c' + a'b'c + a'bc' + abc$	[2 + 5]
3.		Use an appropriate algorithm to determine the product of $(-11)_{10} \times (8)_{10}$ and neatly tabulate each cycle.	[10]
4.		Write a Verilog code to subtract two numbers A = 4'b0101 and B = 4'd2 using adder instantiations.	[10]
5.		In Cheran express, between Coimbatore and Chennai we have only 6 tatkal tickets available under second AC category. Construct a digital circuit using T flip flop which intimates the Railway employee (who books the ticket in the railway station) when the seats are full, by an output signal.	[15]
		Total Marks	[50]

⇔⇔⇔