Reg. No.: 21BCE1696

Name : Vishal

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Vellore Institute of Technology

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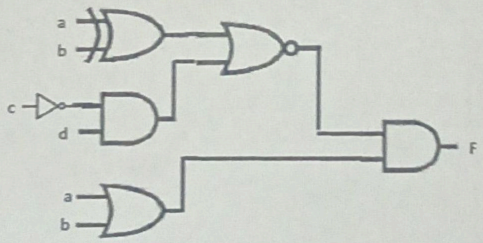
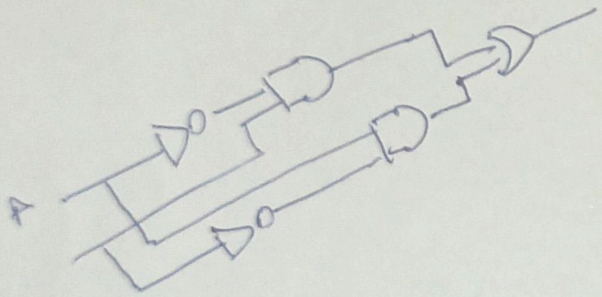
Continuous Assessment Test I – September 2022

Programme	:	B.Tech ECE/ECM	Semester	:	FS 2022-23
Course	:	Digital System Design	Code	:	BECE102L
			Class Nbr	:	CH2022231001853
Faculty	:	Dr.E.Manikandan	Slot	:	E1+TE1
Time	:	90 Minutes	Max. Marks	:	50

Answer ALL the questions

Q.No.	Sub-division	Question Text	Marks
1.		a) Reduce the following Boolean expressions WXY'Z+W'XZ+WXYZ b) Express the given function as in a) in POS form	[2] + [3]
2.		F(A,B,C,D)= π(1,4,6,12,14) i) Simplify the given Boolean function in SOP form using K-Map. ii) Draw a CMOS logic circuit for this simplified expression. (Assume both true and complementary inputs are available)	[5] + [5]
3.		Consider the combinational circuit shown  Determine the truth table for the output F as a function of the four inputs.	[5]
4.		Simplify the given function and for the simplified expression write the Verilog program using (a)Behavioral and (b) dataflow modelling. $F1 = \sum(1,2,3,6,8,9,10,12,13,14)$.	[10]
5.		Identify the errors in the Verilog program given below for the Boolean expression $F = (A + \underline{CD})(\underline{A} + B)$. *Module test (a, b, c, d, F)* *input a,b,c,d;* *output F;*	[10]

		reg f1,f2,f3,f4; *not g1(f1,a);* *nand g2(f2,c,d);* *or g3(f1,f3,b);* *or g3(f4,a,f2);* *nand (F, f3,f4)* *end module* Check for both syntactic and logical errors, Correct it.	
6.		Design a full-subtractor circuit and implement the same a) using a suitable decoder. b) using NAND only	[10]
		Total Marks	[50]



$\bar{A}B + A\bar{B}$

$\overline{A \cdot B}$